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1. Field of the Invention The present invention relates to a semiconductor memory device and a method of controlling the same, and more particularly, to a semiconductor memory device and a method of controlling the same, which may reduce current consumption in a standby state.

2. Description of the Related Art As the size of semiconductor memory devices decreases due to the development of semiconductor manufacturing technology, the operation of a memory cell and the current consumption of a stand-by mode of a dynamic random access memory (DRAM) have increased. A power supply circuit for supplying power to a sense amplifier and a peripheral circuit for a DRAM uses a switching regulator, and a stand-by mode of the DRAM includes a standby mode and a power down mode. If a power is shut off at a time of the standby mode, a state of a flip-flop memory cell, which is a memory cell for storing data, is not maintained. Since the shut off of the power supply leads to a significant loss of data in a memory cell, the level of the data to be maintained in the memory cell must be higher than the level of the data stored in the memory cell at the time when the shut off of the power supply occurs. The level of data to be maintained in the memory cell may be increased by increasing the size of the memory cell. However, reducing the size of the memory cell decreases the area of the memory cell. Thus, in the present day technology, it is difficult to provide high levels of data to be maintained in the memory cell. A memory system according to an embodiment of the present invention provides a memory cell and a method of controlling a current consumption of a memory cell in a stand-by state. The memory system includes a semiconductor memory device, which includes a memory cell having a high data level maintained in a memory cell transistor in response to a first control signal, a first current source connected to a word line which is selected by the first control signal, a first transistor having a source connected to a second current source, a first node, a gate connected to a

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